Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NECD557	On-Chip Interconnects	3	0	0	3

Course Objective

To provide in depth knowledge of interconnect modeling and performance analysis; introduction and analysis of futuristic material based interconnects such GNRs, CNTs and so on

Learning Outcomes

At the end of the course, the student must be able to

- quantify the significance of interconnects in IC Design
- understand the role of repeaters
- get an insight on Transmission line parameters of VLSI interconnects
- understand the novel solutions on interconnects

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Moore's Law, Technological trends, ITRS; Interconnect dimensions, 3D-interconnect, definition of pitch, concept of sheet resistance as applicable for interconnects; Aluminum interconnects, fabrication techniques, Electromigration, Hillock formation, Junction Spiking; Copper Interconnect and low-k dielectric materials. Damascene process, Electroplating and CMP	7	This section introduces the subject and marks the importance of the subject in semiconductor industry, with emphasis on the fabrication aspects.
2	Interconnect resistance and capacitance; Distributed model of interconnect, single and multi rung ladders, RC time delay, Elmore's delay; Local and Global interconnect, interconnect length prediction – Rent's rule and parameters; Interconnect scaling (local and global): ideal, quasi-ideal, constant-R, constant dimension.	8	This module emphasizes on how to cope with interconnect parcitics which impose severe restrictions in circuit performance. The students will also come to know the importance of scaling, as applicable to interconnects.
3	Analytical model of delay using lumped and distributed parameters; Repeater design and optimization.	6	This section focuses on the delay models of interconnects and methods for its improvement, with emphasis on repeater design.
4	Inductive parasitic: Effect of inductance, transmission line model of interconnects; skin effect and its influence on resistance and inductance; Output drivers, reduced-swing circuits and advance interconnect techniques.	7	This section deals with the qualitative and quantitative visualization of interconnects as transmission lines
5	Cross-Talk: Theoretical basis of modeling cross-talk, capacitive and inductive matrix, power distribution noise	7	Students here will come to know about cross-talk and methods for minimizing the same
6	Emerging on-chip interconnects: CNT, Graphene, optical interconnects and so on	7	This deals with the emerging materials that can be used as on-chip interconnects.
	Total	42	

Textbook:

1. H. B. Bakoglu, "Circuits, Interconnections, and Packaging for VLSI", Addison-Wesley Publishing Company
2. Jan M. Rabey, A. Chandrakasan and B. Nikolic , "Digital Integrated Circuits – A design perspective", PHI.
3. Sung-Mo Kang & Yusuf Lablebici, "CMOS Digital Integrated Circuits, Analysis & Design", TMH Edition..

Reference Books:

1. High-Speed VLSI Interconnects, Ashok K. Goel, John Wiley & Sons, 2007.
2. Selected journal papers/IEEE.